```
L1          45 S ((NORMAL OR GOOD) (P) (DEFECTIVE OR FAULTY) (P) SELECT?
(P)
L2           5 S L1 AND 395/CLAS
L3           3 S (5602987 OR 5297148 OR 5095344)/PN
L4           0 S L1 AND L3
L5          12 S L1 AND 371/CLAS
L6          10 S L5 AND 365/CLAS
L7          15 S L3 OR L5 OR L6
L8          22 S ((NORMAL OR GOOD) (P) (DEFECTIVE OR FAULTY) (P) SELECT?
(P)
L9           4 S L8 AND L7
```

US PAT NO: 4,989,181 [IMAGE AVAILABLE] L9: 3 of 4
DATE ISSUED: Jan. 29, 1991
TITLE: Serial memory device provided with high-speed address control circuit

INVENTOR: Moemi Harada, Tokyo, Japan
ASSIGNEE: NEC Corporation, Tokyo, Japan (foreign corp.)

APPL-NO: 07/358,112
DATE FILED: May 30, 1989
FRN-PRIOR: Japan 63-133453 May 30, 1988
INT-CL: [5] G11C 8/00
US-CL-ISSUED: 365/200, 240; 371/10.2
US-CL-CURRENT: 365/200, 240; 371/10.2
SEARCH-FLD: 365/200, 230.05, 239, 240, 221; 371/10.2

REF-CITED:
U.S. PATENT DOCUMENTS
4,701,887 10/1987 Ogawa 365/200

ART-UNIT: 233
PRIM-EXMR: Joseph A. Popek
LEGAL-REP: Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT:
A semiconductor memory device having a serial access port and an improved redundant structure which can operate at a high speed is disclosed. The memory device comprises a normal memory cell array, a redundant memory cell array, a serial selection circuit for serially selecting data stored in the normal cell array in response to a control signal, a defective location memory for storing address of a defective memory cell or cells in the normal memory cell array, a counter incremented by the control signal for indicating the address selected by the serial selection circuit, a control circuit for selecting the redundant memory cell array when the content of the counter coincides with the content of the defective location memory, a plus-one circuit for generating an initial address which is larger than external initial address by one, and a count-up control circuit for applyig the control signal to the counter from its second occurrence after the application of the external initial address.
5 Claims, 7 Drawing Figures

L9: 4 of 4

US PAT NO: 4,475,194 [IMAGE AVAILABLE]
DATE ISSUED: Oct. 2, 1984
TITLE: Dynamic replacement of defective memory words
INVENTOR: Russell W. LaVallee, Poughkeepsie, NY
Philip M. Ryan, Hopewell Junction, NY
Vincent F. Sollitto, Jr., Rhinebeck, NY
ASSIGNEE: International Business Machines Corporation, Armonk, NY (U.S. corp.)
APPL-NO: 06/363,700
DATE FILED: Mar. 30, 1982
INT-CL: [3] G11C 11/40
US-CL-ISSUED: 371/10; 364/200; 365/200; 371/11, 38
US-CL-CURRENT: 371/10.2; 364/232.7, 238.4, 243, 245, 245.3, 265.3, 265.4, 285, DIG.1; 365/200
SEARCH-FLD: 371/10, 11, 13, 38; 365/200, 230; 364/200, 900
REF-CITED:

U.S. PATENT DOCUMENTS

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4,150,428	4/1979	Inrig et al.	371/10
4,310,901	1/1982	Harding et al.	371/10
4,376,300	3/1983	Tsang	371/10

ART-UNIT: 236
PRIM-EXMR: Jerry Smith
ASST-EXMR: M. Ungerman
LEGAL-REP: Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT:
A single error correcting memory is constructed from partially good components on the design assumption that the components are all-good. Those small number of logical lines containing double-bit errors are replaced when detected with good lines selected from a replacement area of the memory. The replacement area is provided by a flexibly dynamically deallocated portion of the main memory so that it can be selected from any section of the original memory by inserting the appropriate page address in the replacement-page register. With such a memory architecture until the first double-bit error is detected (either in testing or actual use) all pages may be used for normal data storage. When such an error is detected some temporarily unused page in the memory is deal-located, that is rendered unavailable for normal storage, and dedicated to providing substitute lines. The same procedure is followed for subsequent faults. If the replacement area itself becomes defective, a different page may be chosen to provide substitute lines simply by providing a different address in the replacement page register.

8 Claims, 3 Drawing Figures